

The impact of classical electronics constraints on a solid-state logical qubit memory

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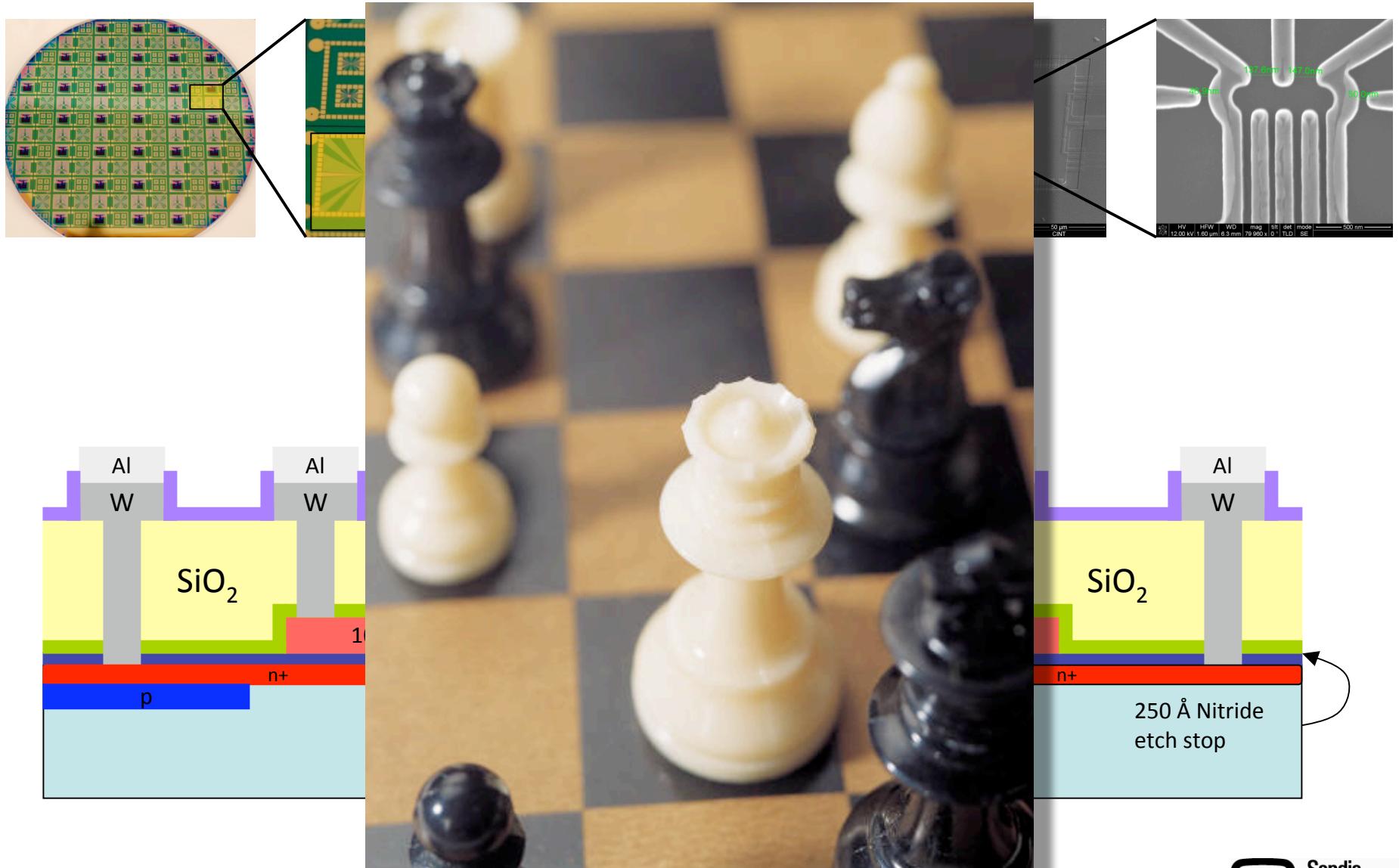
arXiv:0904.0003

J.E. Levy, A. Ganti, C.A. Phillips, B.R. Hamlet, AJL, T.M. Gurrieri, R.D. Carr, M.S. Carroll

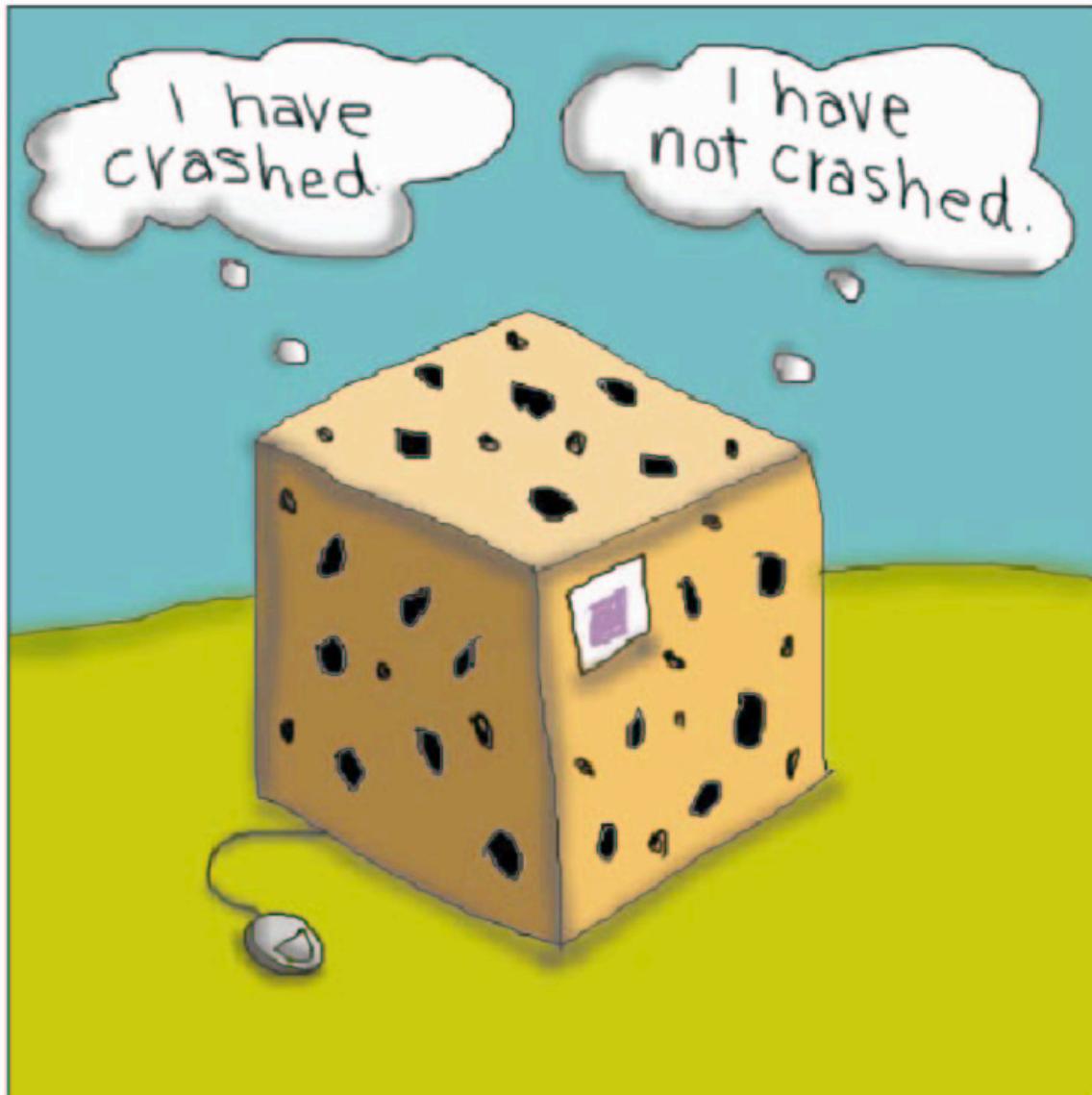
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Si MOS double-quantum-dot (DQD) qubits



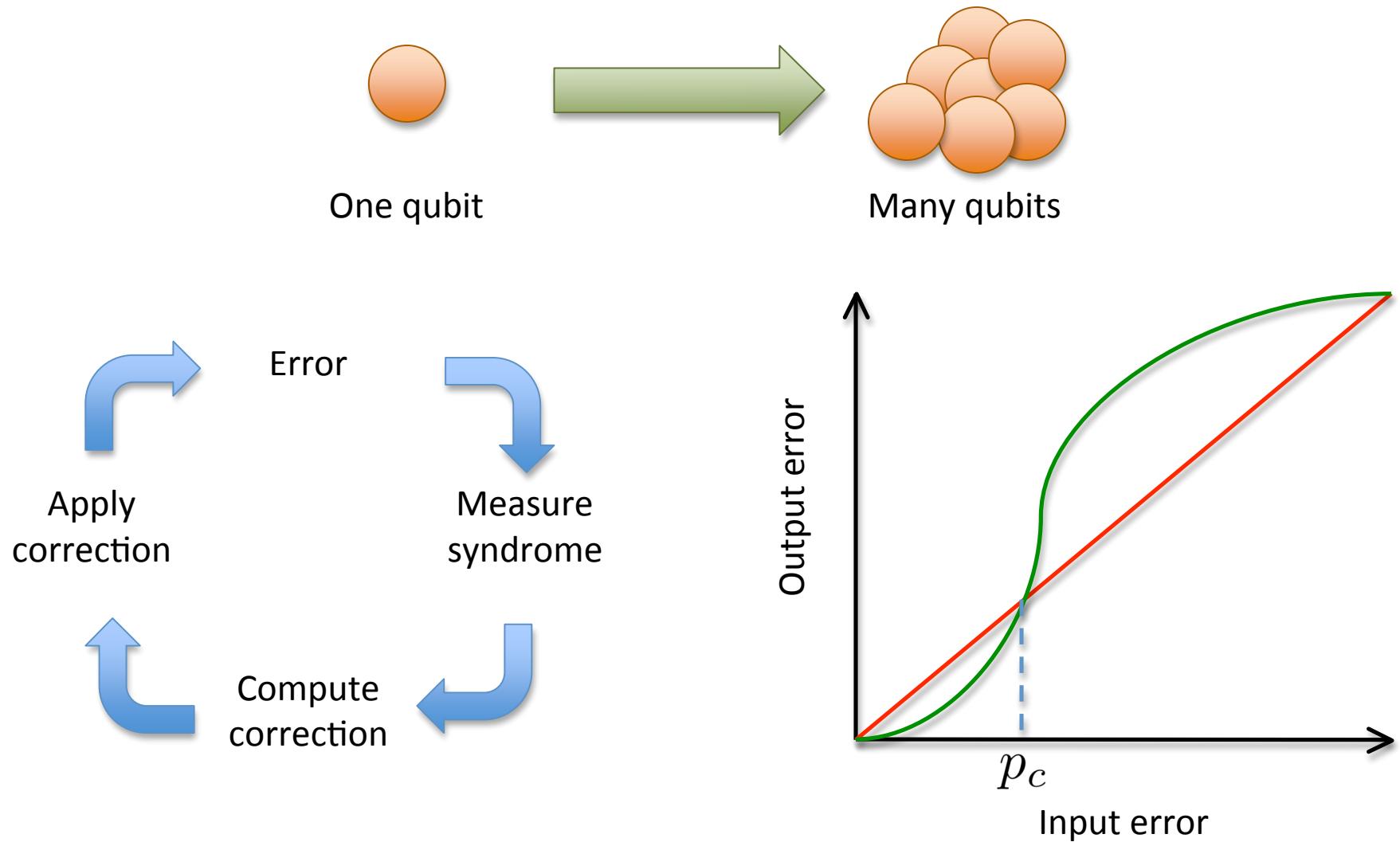
Design an architecture for a task... But what task?



Schrödinger's computer.

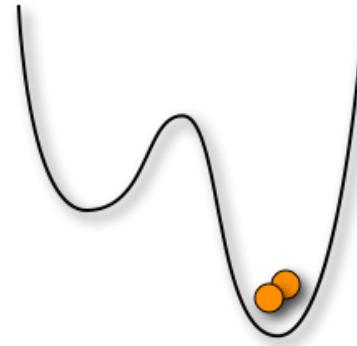
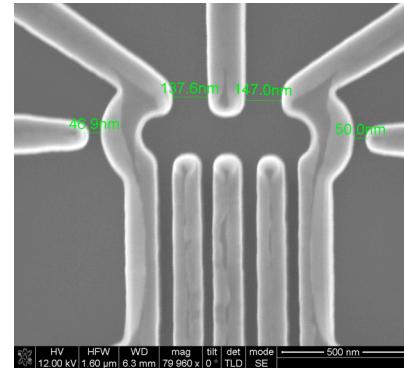
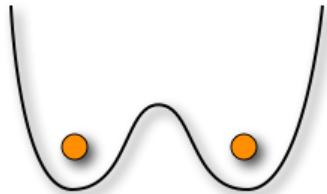
—Sally O. Lee

A logical qubit



Goal: A fault-tolerant architecture for a logical qubit

DQD gates: prepare/measure

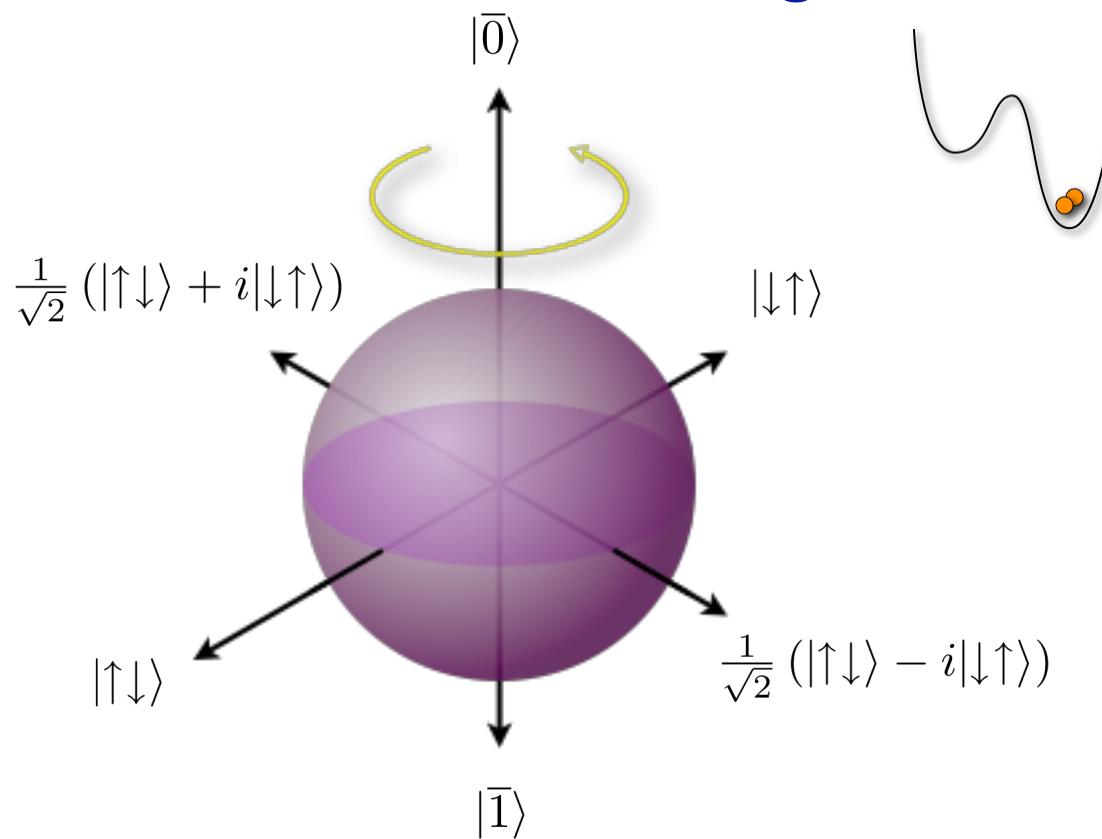


$$|\bar{0}\rangle := |T_0\rangle = \frac{1}{\sqrt{2}}(|\uparrow\rangle_L |\downarrow\rangle_R + |\downarrow\rangle_L |\uparrow\rangle_R)$$

$$|\bar{1}\rangle := |S\rangle = \frac{1}{\sqrt{2}}(|\uparrow\rangle_L |\downarrow\rangle_R - |\downarrow\rangle_L |\uparrow\rangle_R)$$

Main idea: spin-to-charge transduction

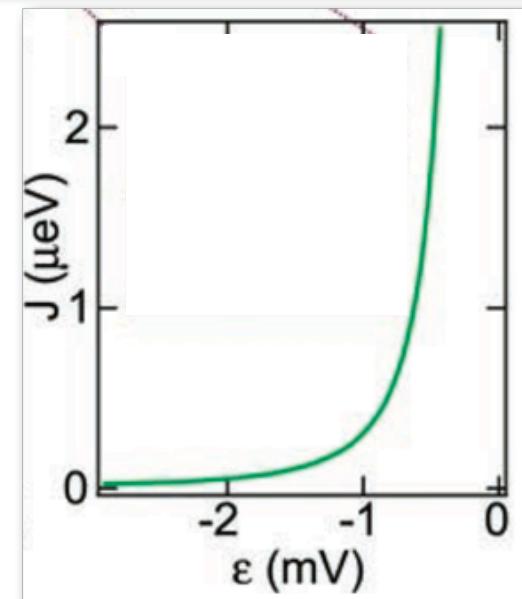
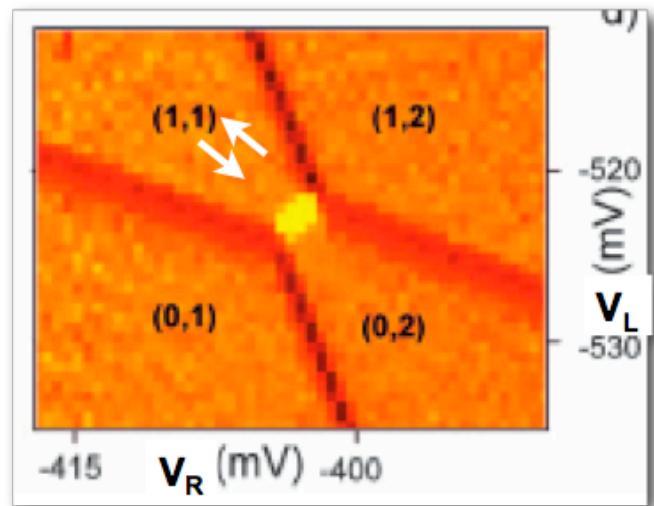
DQD gates: Z-rotations



Driven by effective exchange interaction

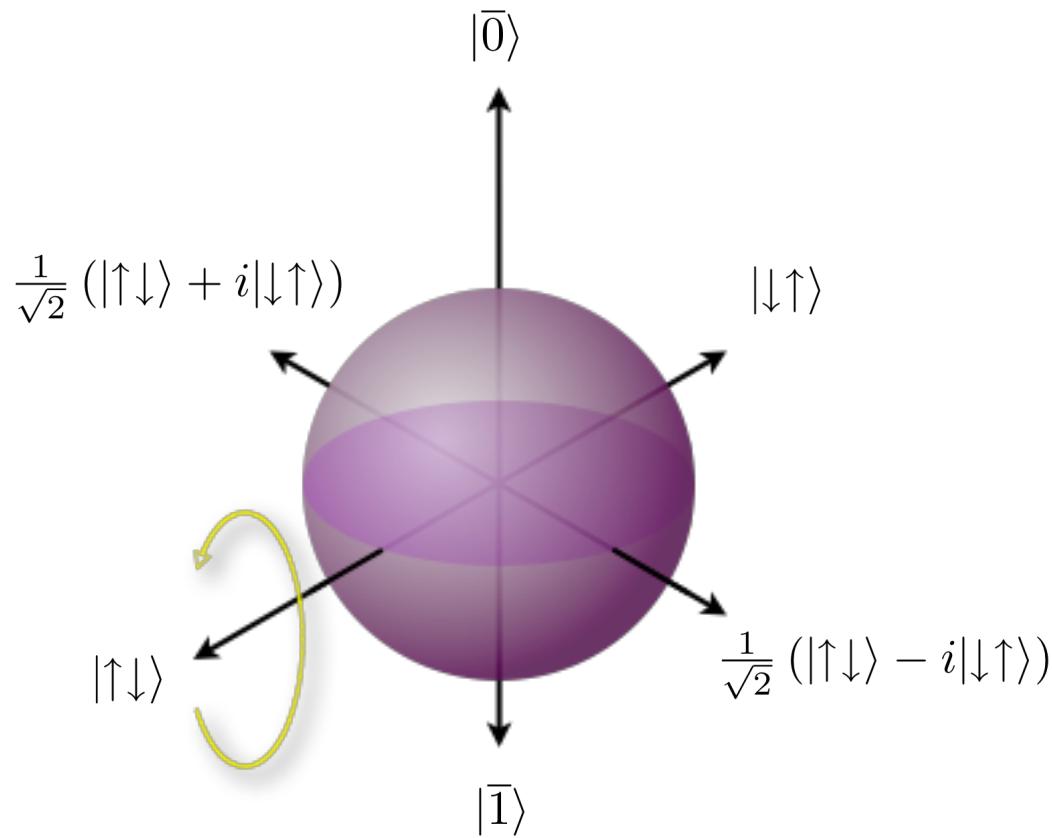
$$H_{eff} = J(X_L X_R + Y_L Y_R + Z_L Z_R)$$

$$\exp(-iH_{eff}t/\hbar) \cong \overline{Z}_{Jt/\hbar}$$



[Petta et al., Science **309**, 2180 (2005)]

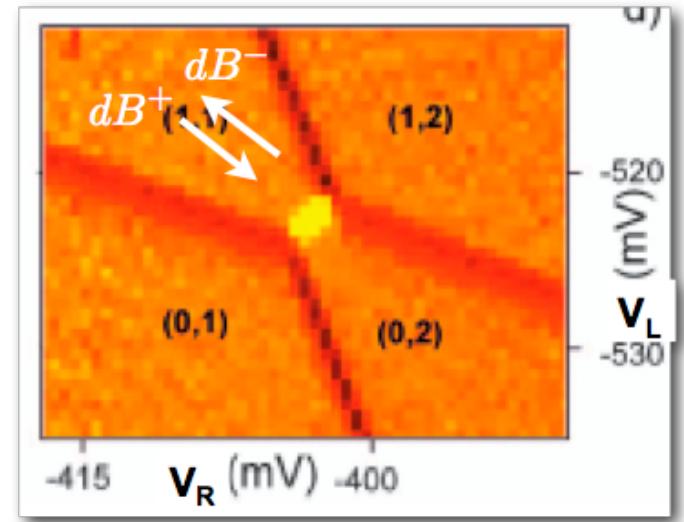
DQD gates: X-rotations



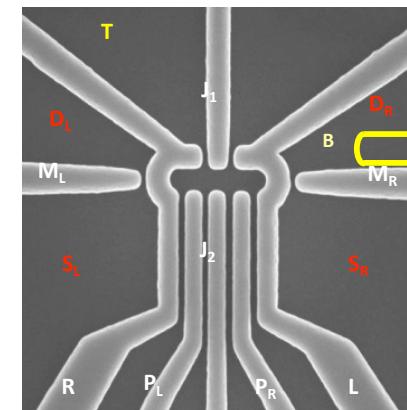
Driven by magnetic field gradient from a local inductor

$$H_{eff} = \mu_B (g_L B_L^z Z_L + g_R B_R^z Z_R)$$

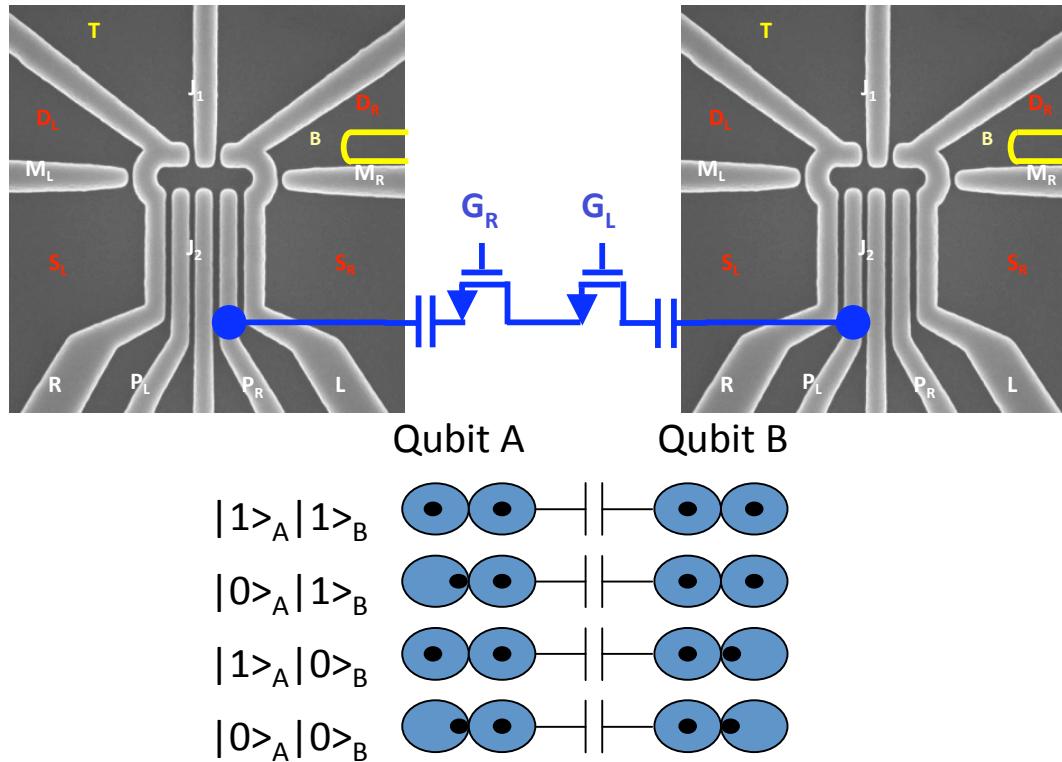
$$\exp(-iH_{eff}t/\hbar) \cong \overline{X}_{\mu_B g dB t/\hbar}$$



[Petta et al., Science 309, 2180 (2005)]



DQD gates: CPHASE



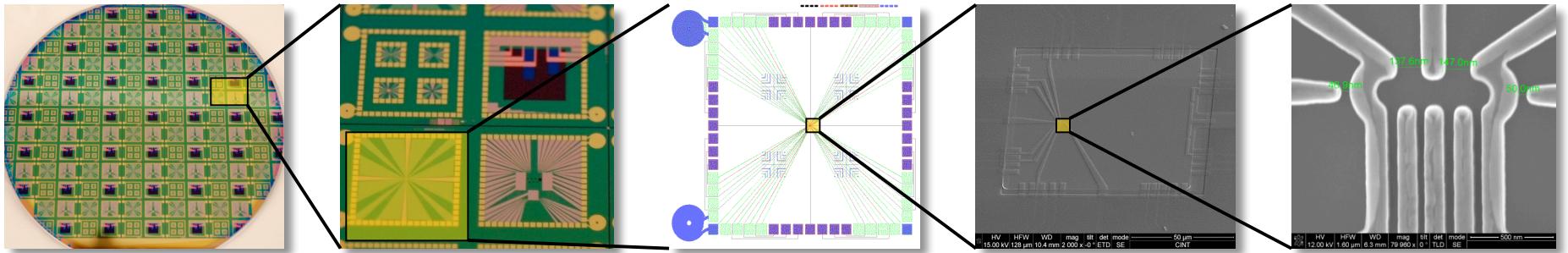
Driven by Coulomb dipole force

$$H_{eff} = \text{diag}(1, 1, 1, J)$$

[Taylor et al., Nat. Phys. 1, 177 (2005)]

$$\exp(-iH_{eff}t/\hbar) \cong \text{diag}(1, 1, 1, e^{-itJ/\hbar})$$

Silicon double-quantum-dot (DQD) qubits



Control constraints

- 2D layout
- 17 wires/qubit
- No qubit transport
- Low temperature (100 mK)
- Limited native gate set

Dynamical decoupling

I^* : raw idle I : protected idle

$$I^* \rightarrow Z \cdot I^* \cdot Z \cdot I^* = I$$

$$\sim 3 \text{ } \mu\text{s} \mapsto \sim 60 \text{ ms}$$

[Tyryshkin et al., PRB **68**, 193207 (2003)]

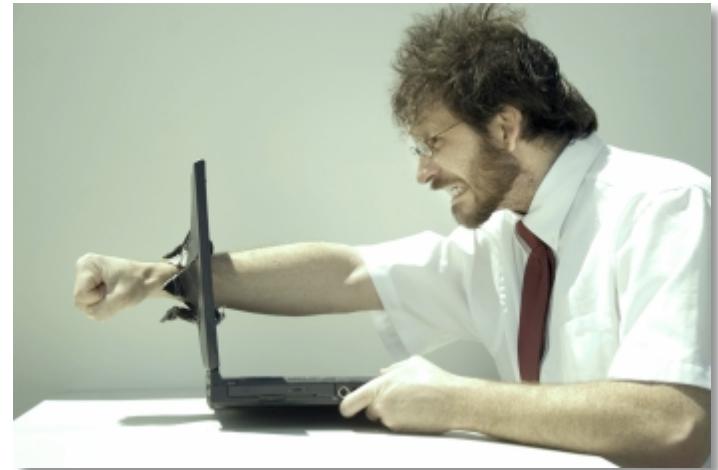
	$M_Z, 1\rangle$	S	Z	$X_{\pi/2}$	$X, CPHASE$	I^*	I
Gate time	τ	τ	2τ	3τ	4τ	τ	τ
Failure probability	$p/30$	p	$2p$	$4p$	$4p$	10^{-2}	5×10^{-7}

} Charge fluctuations } Magnetic fields

Electronics constraints

Power

- Cooling power is limited at 100 mK
- Electronics must be thermally staged



Time

- Electronic timing precision (jitter)
- Limited bandwidth to 100 mK
- 30 ns clock
- Multiplexing used to handle limited parallelism
- Error-correction schedule must be optimized

Space

- Qubit coupling susceptible to crosstalk
- Short 0.5 μm spacing between 1 μm² DQDs
- 65 nm process, 8 metal layers: 3 qubits/controller
(scheduling constraint)

Transport

- No feasible hardware mechanism
- Logical transport very noisy using native gate set
- Local quantum processing only

Local check codes

(a.k.a. Topological quantum codes)

Each syndrome measurement (check) acts
on a constant number of neighboring qubits.

Bacon-Shor codes

[Shor, PRA **52**, 2493 (1995)]

2 qubits per check

[Bacon, PRA **73**, 012340 (2006)]

Kitaev surface codes

[Kitaev, Ann. Phys **303**, 2 (2003)]

4+ qubits per check

[Bombin, Martin-Delgado, PRA **76**, 012305 (2007)]

Color codes

[Bombin, Martin-Delgado, PRL **97**, 180501 (2006)]

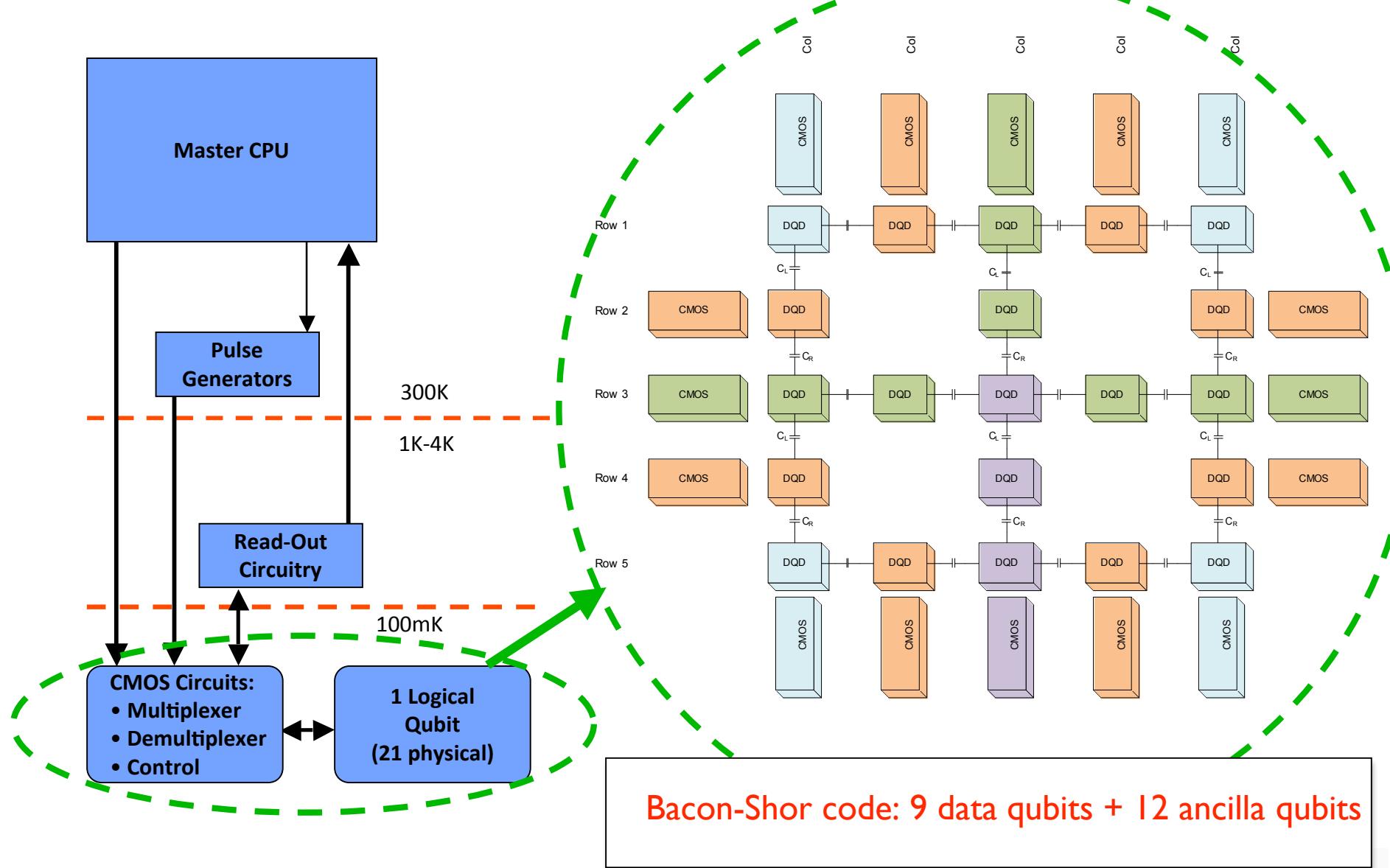
4+ qubits per check

Repetition code

[Aliferis, Preskill, PRA **78**, 052331 (2008)]

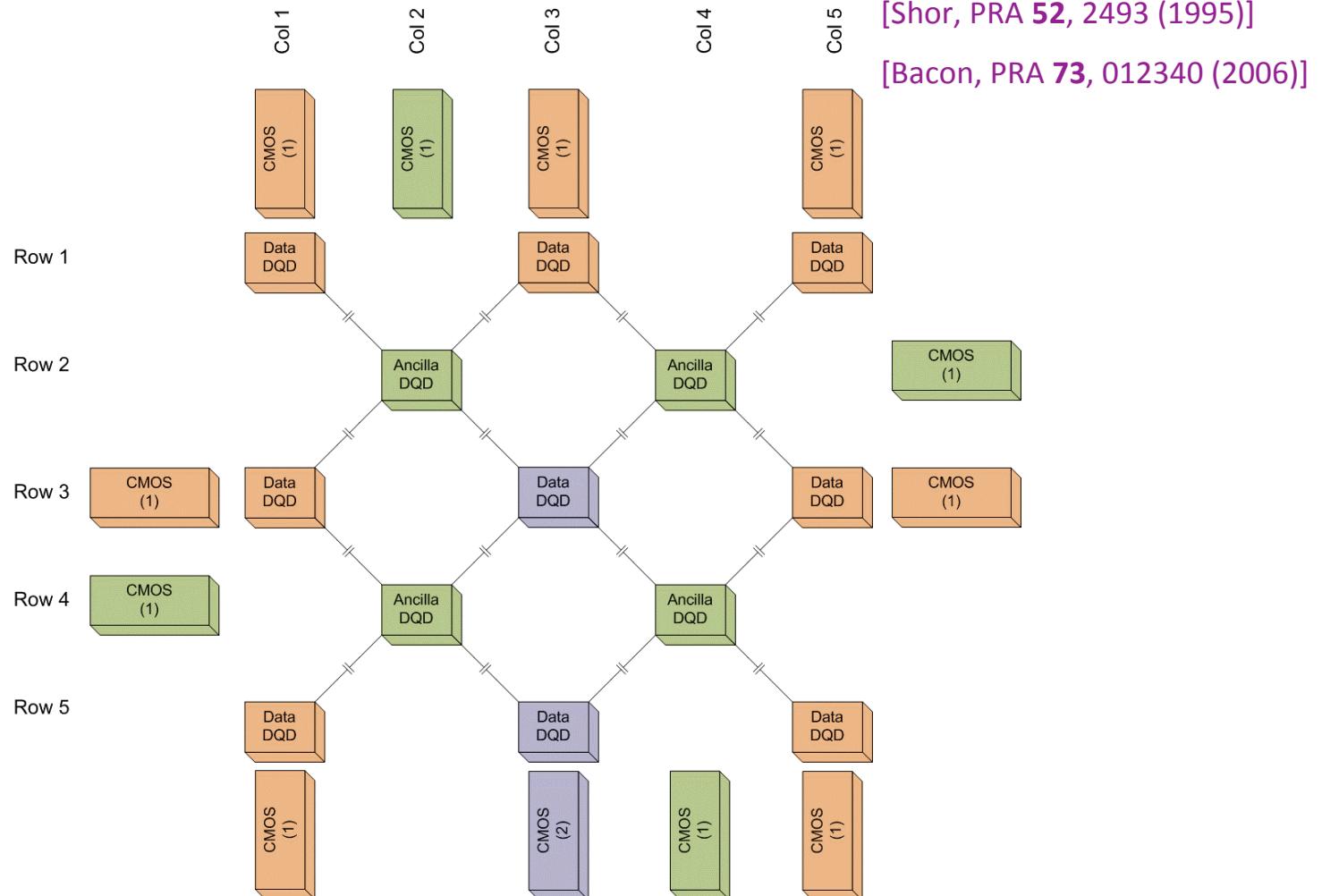
2 qubits per check (bit-flip or
phase-flip only)

Architectural design



[Shor, PRA **52**, 2493 (1995)] [Bacon, PRA **73**, 012340 (2006)]

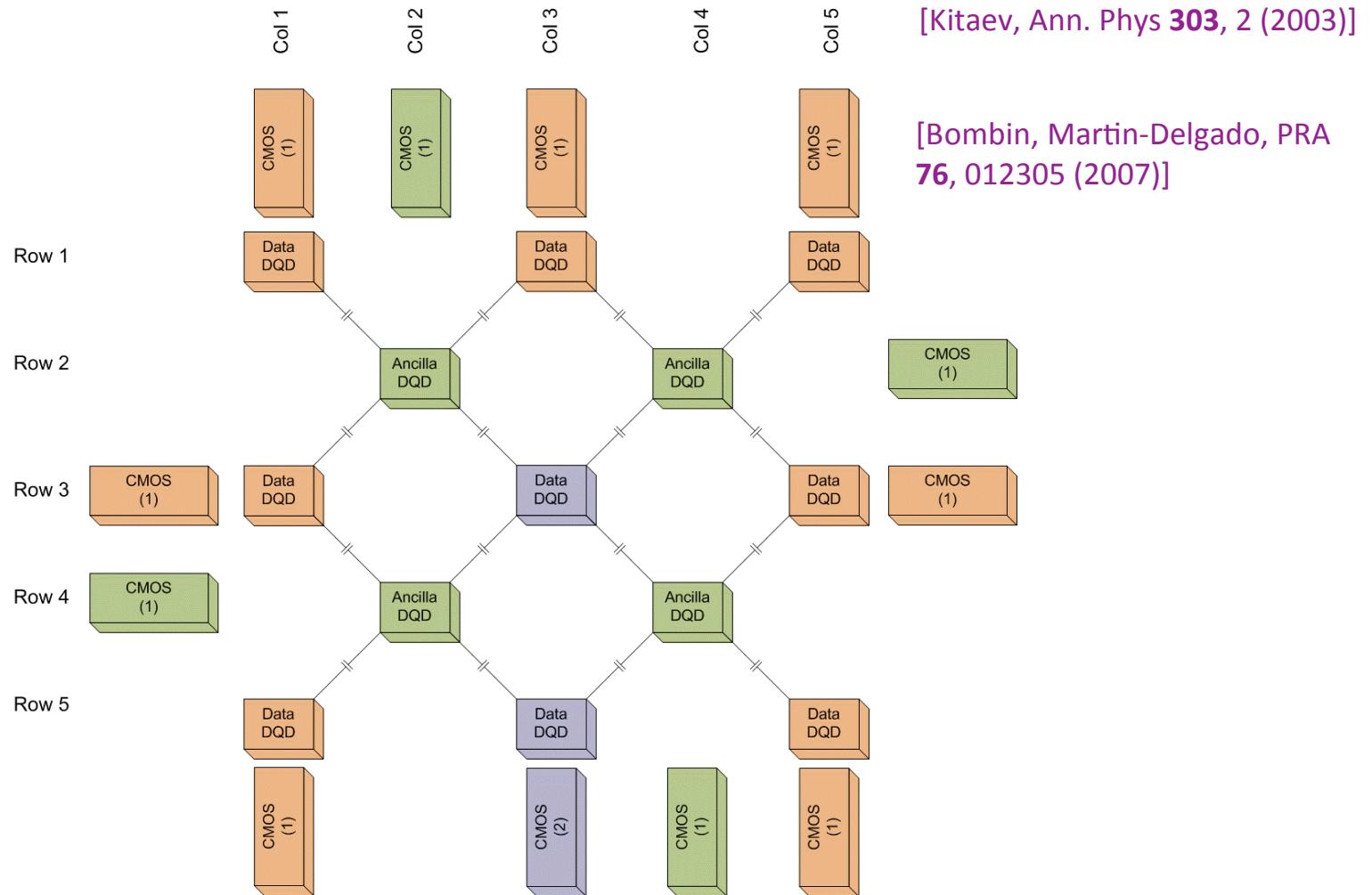
Bacon-Shor code with only 4 ancilla



[Shor, PRA 52, 2493 (1995)]

[Bacon, PRA 73, 012340 (2006)]

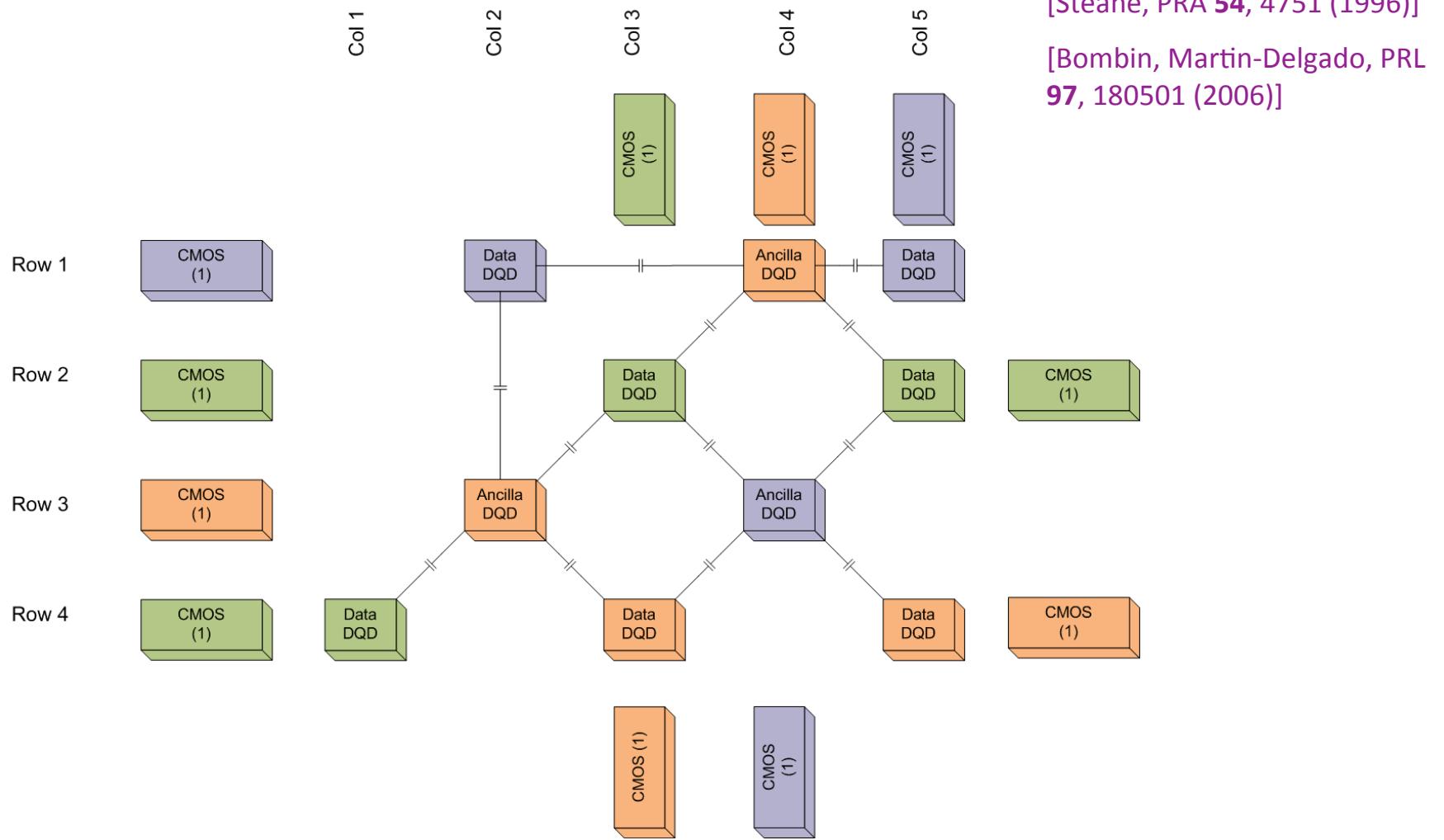
Smallest surface code



[Kitaev, Ann. Phys **303**, 2 (2003)]

[Bombin, Martin-Delgado, PRA **76**, 012305 (2007)]

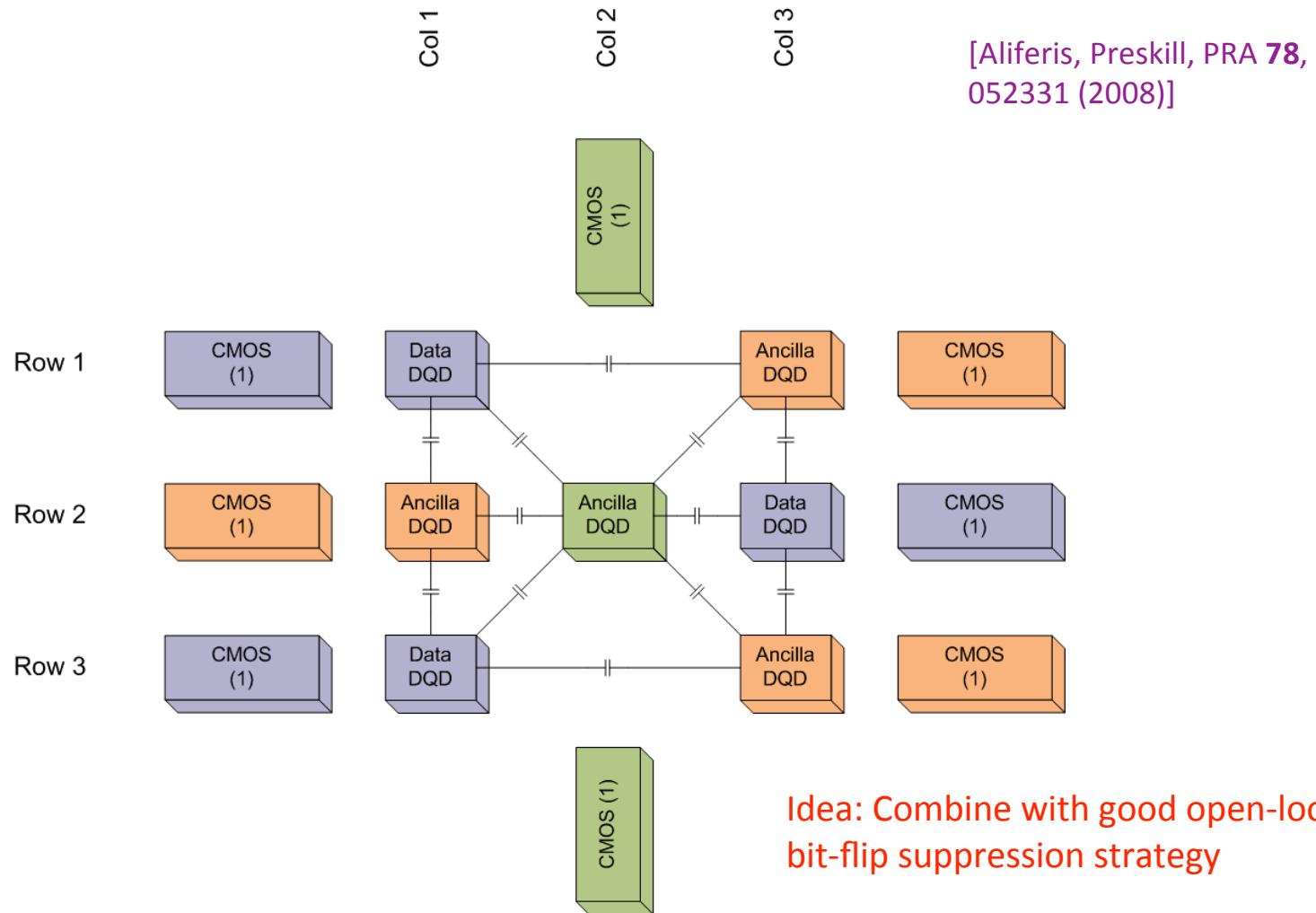
Smallest color code (Steane code)



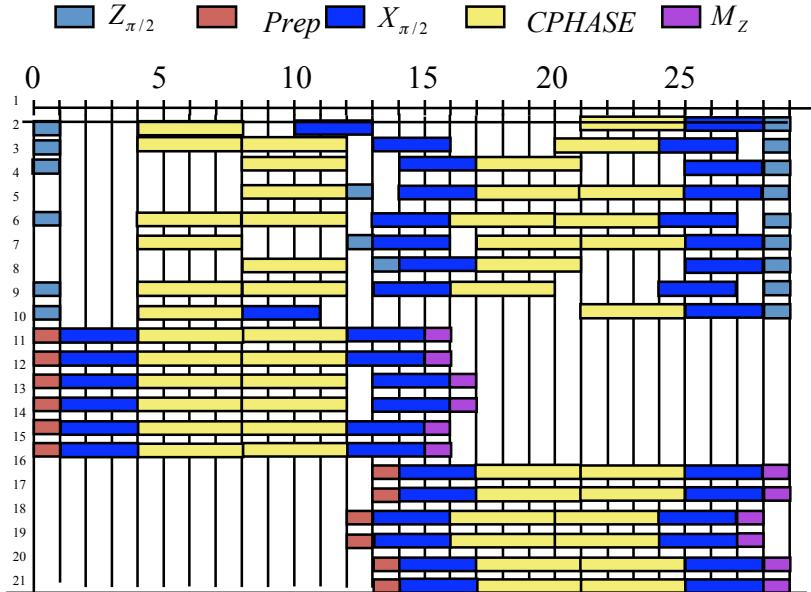
[Steane, PRA 54, 4751 (1996)]

[Bombin, Martin-Delgado, PRL 97, 180501 (2006)]

Smallest repetition code

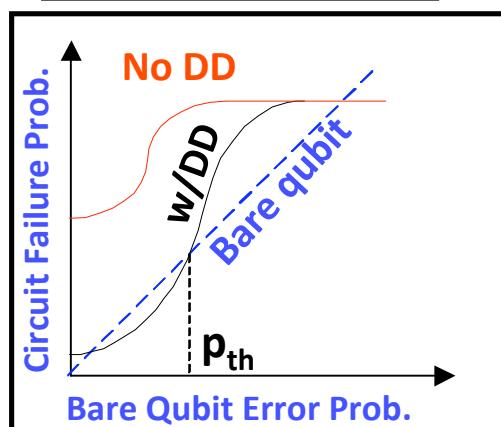


Results for Bacon-Shor code (12 ancilla)



Idle-minimizing schedule (integer program)

Quantum Circuit Performance



	$M_Z, 1\rangle$	S	Z	$X_{\pi/2}$	$X, CPHASE$	I^*	I
Gate time	τ	τ	2τ	3τ	4τ	τ	τ
Failure probability	$p/30$	p	$2p$	$4p$	$4p$	10^{-2}	5×10^{-7}

Gate	IP-optimized	Hand-generated
	BS9(21) w/o DD	BS9(21) with DD
Prep $ 1\rangle$	12	12
$X_{\pi/2}$	42	42
$Z_{\pi/2}$	18	18
X	0	104
CPHASE	24	24
M_Z	12	12
I / I^*	95	219

DD: more idles, but lower idle error rate

- Without DD: idle error is 1×10^{-2}
- With DD: idle error is 5×10^{-7}

Native gates, optimal schedule	Native gates, DD, suboptimal schedule
No Threshold	$2.0 \pm 0.1 \times 10^{-5}$

Cf. 1.94×10^{-4} in [Aliferis, Cross, PRL **98**, 220502 (2007)]

where circuits are considered but constraints are ignored.

Comparative code results (New!)

No architectural considerations
(except locality)

Code (Data)	Threshold
Bacon-Shor 9	1.1×10^{-2}
Kitaev 13	1.4×10^{-2}
Steane 7 (Color Code)	1.9×10^{-2}
Kitaev-Bombin 9	2.7×10^{-2}

With architectural considerations

Code with DD Data(Data+Ancilla)	Threshold
Kitaev-Bombin 9(13)	9.4×10^{-6}
Bacon-Shor 9(21)	2.0×10^{-5}
Bacon-Shor 9(13)	1.4×10^{-4}
Steane 7(10)	4.6×10^{-4}
Repetition 3(7)	1.1×10^{-3}

Smallest local check codes that encode one (logical) qubit in many (data) qubits and correct for an arbitrary single-qubit error

Hand-optimized schedules
 $T_2 = 60$ ms (decoherence time)
 $\tau = 30$ ns (gate time)
Noise = bit-flip (T_2) followed by phase-flip (p)

	$M_Z, 1\rangle$	S	Z	$X_{\pi/2}$	$X, CPHASE$	I^*	I
Gate time	τ	τ	2τ	3τ	4τ	τ	τ
Failure probability	$p/30$	p	$2p$	$4p$	$4p$	10^{-2}	5×10^{-7}

Penalty of shared controllers

<i>1 Round of LV</i>	Prep	Idle	X $\pi/2$	Z $\pi/2$	CPHASE	Z	Msr
BS9(21) Z Stabs	6	610	12	0	12	184	6
BS9(13) Z Stabs	6	492	12	0	12	60	6
KB9(13) Z Stabs	4	656	8	0	12	82	4
Stn7(10) Z Stabs	3	194	6	0	12	40	3
BS9(21) X Stabs	6	672	30	18	12	216	6
BS9(13) X Stabs	6	526	30	18	12	76	6
KB9(13) X Stabs	4	450	26	18	12	78	4
Stn7(10) X Stabs	3	124	20	14	12	40	3
Rptn3(7)	6	660	12	12	18	72	6

Aside: Bit-flip channel from single-spin T_2

Single-spin T_2 process is phase-flip channel on electron spins

$$\rho \mapsto (1-p)^2 \rho + p(1-p)(ZI \rho ZI + IZ \rho IZ) + p^2 ZZ \rho ZZ$$
$$p = \frac{1}{2} \left(1 - e^{-t/2T_2} \right)$$

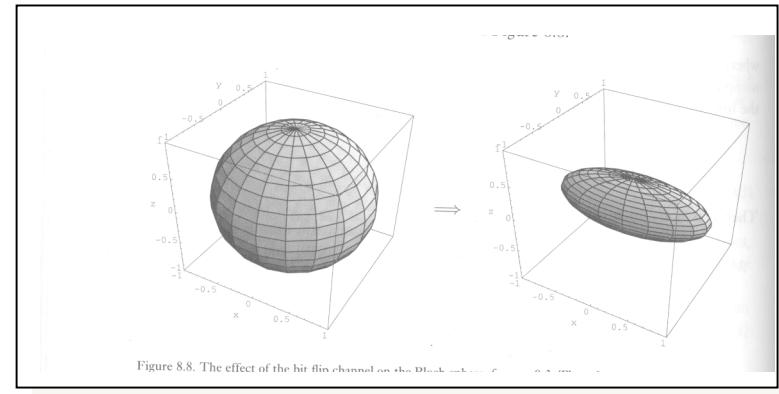
Singlet-triplet encoding is a $[[2,1]]$ stabilizer code

$$|\bar{0}\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)$$

$$\begin{aligned} S_1 &= -ZZ \\ \bar{X} &= ZI \end{aligned}$$

$$|\bar{1}\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)$$

$$\bar{Z} = XX$$

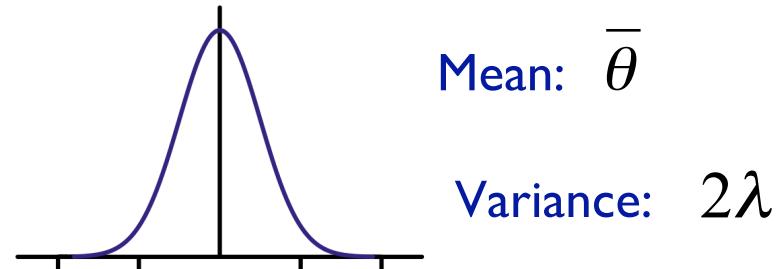


$$\rho \mapsto (1 - p_{eff})\rho + (1 - p_{eff})\bar{X}\rho\bar{X}$$

$$p_{eff} = 2p(1-p)$$

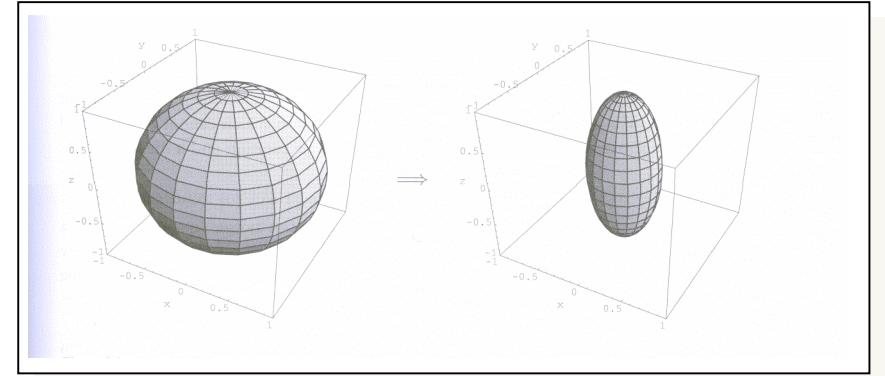
Aside: Phase-flip channel on Z Gates

$$\rho \mapsto \int d\theta p(\theta) Z_\theta \rho Z_{-\theta}$$



$$p(\theta) = \frac{1}{\sqrt{4\pi\lambda}} e^{-(\theta - \bar{\theta})^2 / 4\lambda}$$

Factoid: $Z_\theta = I \cos \frac{\theta}{2} - i Z \sin \frac{\theta}{2}$



$$\rho \mapsto \underbrace{\left(\int d\theta p(\theta) \cos^2 \theta \right) \rho}_{1-p} + \underbrace{\left(\int d\theta p(\theta) \sin^2 \theta \right) Z \rho Z}_p$$

$$p = e^{-\lambda/2} \sinh \frac{\lambda}{2}$$

To achieve $p=10^{-4}$, need std. dev. of about 1°